Notice of Allowability	Application No.	Applicant(s)	
	10/726,705	KOYAMA ET AL.	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the 09-21-2004 Election*.

2. ☒ The allowed claim(s) is/are *7-21*.

3. ☒ The drawings filed on *04 December 2003* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 20031204
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20041209* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

SHOUXIANG HU
PRIMARY EXAMINER

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Eckhard H. Kuesters (RN: 28,870) on December 7, 2004.

The application has been amended as follows:

IN THE TITLE

The title is changed as following:

A Method of Forming a Semiconductor Device ~~and Method of Manufacturing the Same~~ Having an Amorphous/crystalline Gate Insulating Layer

IN THE CLAIMS

1-6. (Canceled)

7. (Currently Amended) A method of manufacturing a semiconductor device comprising:

forming an amorphous insulating layer containing metal, silicon and oxygen on a substrate, the amorphous insulating layer further containing nitrogen in a surface region thereof; and

heat-treating the amorphous insulating layer in a non-oxidizing atmosphere, permitting a solid-phase growth to take place in a region containing no nitrogen in the amorphous insulating layer while remaining the nitrogen-containing surface region as an amorphous insulating layer, thereby forming an epitaxial crystalline insulating layer containing [[a]] said metal, silicon and oxygen on and in contact with the substrate ~~side of the amorphous insulating layer~~.

8. (Original) The method of manufacturing a semiconductor device according to claim 7, wherein the nitrogen is contained in the surface region of the amorphous insulating layer at a concentration of 15 atom% or more.

9. (Original) The method of manufacturing a semiconductor device according to claim 7, wherein the metal includes at least one element selected from the group consisting of Zr, Hf, Ti and lanthanoid elements.

10. (Original) The method of manufacturing a semiconductor device according to claim 7, wherein the surface region containing nitrogen has a thickness ranging from 1 nm to 2.5 nm.

11. (Currently Amended) The method of manufacturing a semiconductor device according to claim 7, wherein the amorphous insulating layer containing nitrogen in the surface region thereof is formed by depositing a metal silicate film on the substrate and exposing the metal silicate film to ~~exited~~ excited nitrogen.

12. (Original) The method of manufacturing a semiconductor device according to claim 11, wherein the metal silicate film has a thickness of 10 nm or less.

13. (Currently Amended) The method of manufacturing a semiconductor device according to claim 7, wherein the nitrogen-containing surface region of the amorphous insulating

layer ~~containing nitrogen in the surface region thereof~~ is formed by depositing a metal silicate on the surface in a nitrogen atmosphere.

14. (Original) The method of manufacturing a semiconductor device according to claim 13, wherein the metal silicate film has a thickness of 10 nm or less.

15. (Original) The method of manufacturing a semiconductor device according to claim 7, wherein the non-oxidizing atmosphere is an atmosphere containing oxygen at a partial pressure of 1×10^{-3} Torr or less.

16. (Currently Amended) The method of manufacturing a semiconductor device according to claim 7, further comprising forming an electrode on the amorphous insulating film successively after forming the amorphous insulating film.

17. (Original) The method of manufacturing a semiconductor device according to claim 7, wherein the heat treatment is performed at a temperature ranging from 950°C to 1200°C.

18. (Currently Amended) A method of manufacturing a semiconductor device comprising:

forming an amorphous insulating layer containing metal, silicon and oxygen on a substrate, the amorphous insulating layer comprising a surface region and a substrate side remnant region, the surface region further containing a nitrogen of a first concentration, and the remnant region containing a nitrogen of a second concentration less than the first concentration; and

heat-treating the amorphous insulating layer in a non-oxidizing atmosphere, permitting a solid-phase growth to take place so as to form an epitaxial crystalline insulating layer in the

substrate side remnant region in contact with said substrate while ~~having~~ remaining the first region as an amorphous insulating layer.

19. (Original) The method of manufacturing a semiconductor device according to claim 18, wherein the non-oxidizing atmosphere comprises a partial oxygen pressure of 1×10^{-3} Torr or less.

20. (Currently Amended) The method of manufacturing a semiconductor device according to claim 18, wherein said heat-treating is performed after ~~the non-oxidizing atmosphere is formed by~~ depositing a conductive film on the amorphous insulating layer ~~prior to the step of heat-treating~~.

21. (Original) The method of manufacturing a semiconductor device according to claim 18, wherein the metal includes at least one element selected from the group consisting of Zr, Hf, Ti and lanthanoid elements.

Allowable Subject Matter

Claims 7-21 are allowed.

Reasons for Allowance

The following is an examiner's statement of reasons for allowance: Prior art does not teach or render obvious a method of manufacturing a semiconductor device as defined in the above allowed claims, comprising particularly the steps of: forming an amorphous insulating layer of a metal silicate with higher nitrogen concentration at its upper portion than at its lower portion, and annealing it so as to convert the lower

portion to an epitaxial crystalline insulating layer on and in contact with the substrate while still keeping the upper portion as an amorphous insulating portion.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References A-G are cited as being related to a method of forming an insulating layer comprising a step of nitridation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SH
December 9, 2004

SHOUXIANG HU
PRIMARY EXAMINER